Read times:

L1 cache: 3 cycles

L2 cache: 11 cycles

L3 cache: 25 cycles

Main Memory: 1000 cycles

Put the cache interactions in the proper order (you can use the left column to order your answers, write the letters in order in the boxes at the bottom):

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|  | A. The L2 cache controller determines the cache set, the requested cache tag and the block offset |
|  | B. L2 cache identifies the byte field in the L2 cache cache block and returns it to L1 cache |
|  | C. L2 cache writes the block data, LRU info and cache tag to the cache block |
|  | D. L1 cache identifies the byte field in the L1 cache cache block and returns it to The CPU |
|  | E. L1 cache sends the L2 cache controller a memory address |
|  | F. The L1 cache controller determines the cache set, the requested cache tag and the block offset |
|  | G. L1 cache writes the block data, LRU info and cache tag to the cache block |
|  | H. No L1 cache set tag match |
|  | I. No L2 cache set tag match |
|  | J. L3 cache set tag match |
|  | K. L1 cache checks for an empty block in the set |
|  | L. L2 cache checks for an empty block in the set |
|  | M. The CPU sends the L1 cache controller a memory address |
|  | N. Empty block in L2 cache set |
|  | O. L1 cache receives a block from the L2 cache controller |
|  | P. L2 cache receives a block from the L3 cache controller |
|  | Q. L2 cache circuits determine whether the requested tag is in the set by matching existing cache tags to the tag of the request |
|  | R. L3 cache identifies the byte field in the L3 cache cache block and returns it to L2 cache |
|  | S. The L1 cache Controller determines the least recently used block entry |
|  | T. No empty block in L1 cache set |
|  | U. L3 cache circuits determine whether the requested tag is in the set by matching existing cache tags to the tag of the request |
|  | V. L1 cache circuits determine whether the requested tag is in the set by matching existing cache tags to the tag of the request |
|  | W. The L3 cache controller determines the cache set, the requested cache tag and the block offset |
|  | X. L2 cache sends the L3 cache controller a memory address |

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Based on the hit times show above, how many cycles does this interaction take?